REMARKS

Claims 2-7, 9-14, 16-21, 23-28, and 30-40 are pending in this application. Claims 7, 14, 21, 28, and 35-40 are independent claims. Claims 2-6, 9-13, 16-20, 23-27, and 30-34 are dependent claims.

Claims 2-7, 9-14, 16-21, 23-28, and 30-40 have been rejected. Amendments to claims 21 and 40 are presented herein. Claim 21 has been amended to improve form without changing substance. Formal drawings have been submitted for FIGs. 1, 2, and 5-7. No new matter is being presented, and approval and entry are respectfully requested.

Changes to the Drawings

In numbered paragraph 2 on page 2 of the Office Action, the Examiner indicated that the proposed drawing corrections filed on October 22, 2001 and May 29, 2003 have been approved and that formal drawings are required. Accordingly, replacement figures incorporating the approved corrections are submitted herewith for FIGs. 1, 2, and 5-7. No new matter has been added. Approval and entry of the attached replacement sheets are respectfully requested.

Rejections Under 35 U.S.C. §§ 102 and 103

In numbered paragraph 4 on page 3 of the current Office Action, the Examiner rejected claims 2-4, 7, 9-11, 14, 16-18, 21, 23-25, 28, 30-32, and 35 under 35 U.S.C. § 102(b) as being anticipated by Walker et al. (U.S. Patent No. 4,641,231).

In numbered paragraph 5 on page 3 of the current Office Action, the Examiner rejected claims 3, 4, 7, 9-11, 14, 16-18, 21, 24, 25, 28, 31, 32, and 35-40 under 35 U.S.C. § 102(b) as being anticipated by Wilcox (U.S. Patent No. 5,408,150).

In numbered paragraph 6 on page 3 of the current Office Action, the Examiner rejected claims 3, 4, 6, 7, 9-11, 13, 14, 16-18, 20, 21, 24, 25, 27, 28, 31, 32, and 34-40 under 35 U.S.C. § 102(b) as being anticipated by Chaney (U.S. Patent No. 5,502,610).

In numbered paragraph 7 on pages 3 and 4 of the current Office Action, the Examiner rejected dependent claims 2, 23, and 30 under 35 U.S.C. § 103(a) as being unpatentable over Wilcox or Chaney in view of Walker.

In numbered paragraph 8 on page 4 of the current Office Action, the Examiner rejected dependent claims 5, 12, 19, 26, and 33 under 35 U.S.C. § 103(a) as being unpatentable over Chaney in view of Suzuki et al. (U.S. Patent No. 5,675,482).

Applicants respectfully traverse these rejections for the reasons presented below.

The Invention

Independent claim 7 recites a switching regulator including "a detection circuit that detects when the main switch and the synchronous switch are **simultaneously** turned on" (emphasis added). Independent claims 14, 21, 28, and 35-40 recite similar language.

The detection circuit of the present invention detects when the main switch and the synchronous switch are simultaneously turned on. Although the main switch and the synchronous switch are controlled to alternately turn on, there are situations in which the switches can be simultaneously turned on, unintentionally, if, for example, a user improperly uses a device that includes the switching regulator. Accordingly, the present invention includes a detection circuit that detects a state in which the switches are simultaneously turned on. Referring to FIG. 3, the output of AND gate 542 indicates that the switches are simultaneously turned on when the output signal of the AND gate 542 is high.

For example, in FIG. 3, if the first FET 521 is on and the second FET 523 is off, the AND gate 542 receives a low signal from the driver 535 and a high signal from amplifier 541 and outputs a low signal, indicating that the switches are not simultaneously on. If the first FET 521 is off and the second FET 523 is on, the AND gate 542 receives a high signal from the driver 535 and a low signal from amplifier 541 and outputs a low signal, indicating that the switches are not simultaneously on. However, if the first FET 521 is on and the second FET 523 is also on, the AND gate 542 receives a high signal from the driver 535 and a high signal from amplifier 541 and outputs a high signal, indicating that the switches are simultaneously on. Because FET 521 and FET 523 are in series with one another, either one may be monitored.

The Walker Reference

The Examiner has asserted that the comparators 30 and 32 of Walker disclose the detection circuit of the present invention. However, referring to FIG. 2 of Walker, the comparators 30 and 32 merely operate to alternately turn on the semiconductors G1 and G2 and, thus, operate similarly to the PWM comparator 533 in combination with the amplifier 538 and the triangle wave oscillator 539 of the present invention.

In Walker, if the output of comparator 30, for example, is 0, then semiconductor G1 is conducting. The signal applied to AND gate 60 will then prevent the driver 28 from enabling semiconductor G2. At the comparator 30 and at AND gate 60, it is only known whether semiconductor G1 is actually conducting.

However, while both Walker and the present invention monitor the drive signals of the switches, in the present invention, the second switch is also monitored. Thus, the present invention is able to determine whether the switches are actually conducting.

Although AND gate 60 receives a control signal for semiconductor G2 from line 48, the actual condition of semiconductor G2 is not known. In Walker, the condition of one switch is determined to determine how to control the other switch. Walker prevents both switches from being turned on, but does not detect a condition in which both switches are simultaneously on.

In Walker, the comparators 30 and 32 only monitor the outputs of the drivers 26 and 28, not the switches themselves. The drivers 534 and 535 could be working properly, but if the first switch becomes defective and shorts, both switches could be on. The present invention would be able to detect that both switches are on, but Walker would not. In Walker, if semiconductor G1 becomes defective, the driver 28 will never send an enabling signal to semiconductor G2. Thus, the present invention is more thorough.

Therefore, Applicants submit that the independent claims patentably distinguish over the prior art. Accordingly, Applicants respectfully request reconsideration and withdrawal of the rejections under § 102.

The Wilcox Reference

The Examiner has asserted that the logic circuit 32 of Walker discloses the detection circuit of the present invention. However, similar to Walker, the logic circuit 32 of Wilcox merely operates to alternately turn on the MOSFETS 21 and 22, as shown in FIG. 2 of Wilcox, and, thus, operates similarly to the PWM comparator 533 in combination with the amplifier 538 and the triangle wave oscillator 539 of the present invention.

In Wilcox, when input terminal 31 is low, for example, the bottom MOSFET 22 is driven only when the gate-to-source voltage of the top MOSFET 21 (V_{TG}-V_{TS}) is below a predetermined threshold value. In other words, the drive to the bottom MOSFET 22 is inhibited until the top MOSFET 21 is substantially turned off. See Wilcox at col. 4, line 41 to col. 5, line 39. Thus, similar to Walker, Wilcox prevents both switches from being on, but will not detect a condition in which both switches are simultaneously on.

Therefore, Applicants submit that the independent claims patentably distinguish over the prior art. Accordingly, Applicants respectfully request reconsideration and withdrawal of the rejections under § 102.

The Chaney Reference

The Examiner has asserted that the inhibiting circuits 27H and 27L of Chaney disclose the detection circuit of the present invention. However, similar to Walker and Wilcox, the inhibiting circuits 27H and 27L of Chaney merely operate to alternately turn on the transistors 16H and 16L, as shown in FIG. 1 of Chaney, and, thus, operate similarly to the PWM comparator 533 in combination with the amplifier 538 and the triangle wave oscillator 539 of the present invention.

The inhibiting circuit 27H provides an input signal to NAND gate 50L depending on the state of transistor 16H, and inhibits the turning on of transistor 16L until after the transistor 16H gate voltage is below 1.4V. See Chaney at col. 4, lines 1-42. Chaney inhibits the turning on of one transistor until the other transistor is off and does not actually determine whether both are on. Thus, like Walker and Wilcox, Chaney uses the condition of one transistor to determine whether to turn on the other transistor, but Chaney does not detect a condition in which both transistors are on simultaneously.

While column 2, lines 5-8 of Chaney state that the "inhibiting circuit detects the states of the FETs," the inhibiting circuit does not monitor both FETs. Column 2, lines 39-43 of Chaney, states that the inhibiting circuits 27H and 27L "monitor the states of **respective** transistors 16H and 16L" (emphasis added). Thus, each inhibiting circuit 27H and 27L monitors the state of only one of the transistors.

Therefore, Applicants submit that the independent claims patentably distinguish over the prior art. Accordingly, Applicants respectfully request reconsideration and withdrawal of the rejections under § 102.

The Dependent Claims

The dependent claims depend from the above-discussed independent claims and are patentable over the prior art for at least the reasons discussed above.

Examiner Interview

On April 21, 2004, the undersigned conducted an Examiner Interview with Examiner Sterrett. The above arguments were briefly discussed in the Examiner Interview.

The Examiner did not make any commitments during the Examiner Interview. However, the Examiner indicated that he would reconsider the subject application after a Response is filed that includes the above-described remarks.

Conclusion

It is submitted that none of the references, either taken alone or in combination, teach the present claimed invention. Thus, claims 2-7, 9-14, 16-21, 23-28, and 30-40 are deemed to be in a condition suitable for allowance. Reconsideration of the claims and an early Notice of Allowance are earnestly solicited.

If there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

Finally, if there are any additional fees associated with filing of this response, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

STAAS & HALSEY LLP

Date: 5/3/04

By: C. Joan Gilsdorf
Christine Joan Gilsdorf
Registration No. 43,635

1201 New York Avenue, N.W.
Suite 700
Washington, D.C. 20005
Telephone: (202) 434-1500
Facsimile: (202) 434-1501